REMARKS/ARGUMENTS

This Amendment is being filed in response to the Final Office Action dated July 20, 2009. Reconsideration and allowance of the application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1-12 are pending in the Application. Claims 1 and 12 are independent claims. By means of the present amendment, the claims are amended to clarify that which is recited in the claims and to correct clerical errors that introduced inadvertent changes to the claim language. Specifically, claim 1 is amended to clarify the claim parsing such that it is clear that the (emphasis added) "plurality of first and second column conductors, [are] each arranged for inputting data signals to or outputting data signals from the matrix elements ... in first time periods, and [are] each arranged for providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods ..."

Claims 4, 7 and 11 are amended to correct an inadvertent change in the claim introduced by the amendment submitted on April 20, 2009.

By these amendments, claims 1, 4, 7 and 11 are not amended to address issues of patentability and Applicant respectfully reserves all rights under the Doctrine of Equivalents. Applicant furthermore reserves the right to reintroduce subject matter

deleted herein at a later time during the prosecution of this application or continuing applications.

The amendment to claims 1, 4, 7 and 11 are not intended to narrow the scope of the prior claims and are merely submitted to further prosecution of this matter and to either promote allowance of the claims or at least, reduce pending issues and place the claims in better form for appeal. Accordingly, consideration and entrance of the amendment to claims 1, 4, 7 and 11 is respectfully requested.

In the Office Action, claims 1-12 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,712,652 to Sato ("Sato") in view of U.S. Patent No. 6,307,532 to Aoki ("Aoki"). The rejection of claims 1-12 is respectfully traversed. It is respectfully submitted that claims 1-12 are allowable over Sato in view of Aoki for at least the following reasons.

Sato shows a (emphasis added) "liquid crystal display device, comprises: a switch element array substrate (301) having a plurality of data lines (1) and a plurality of scanning lines (2) both arranged being intersected to each other in a matrix form so as to form matrix intersection points; a plurality of pixel electrodes (3) each arranged for each matrix intersection point; and a plurality of first switching elements (6, 7) each arranged for each matrix intersection point and each turned on or off by the scanning line, for applying write voltage supplied from the data

line to the pixel electrode, respectively when turned on ..." (See, Sato, Abstract.)

The Final Office Action takes a position that in Sato (emphasis added), "the first column conductors supply first voltage and the second column conductors supply second voltage to each matrix element and wherein the first voltage and the second voltage are separate voltages ..." (See, Final Office Action, page 3, second paragraph.)

The Applicants respectfully point out that in Sato, the voltages applied by the first and second column conductors are the data signal voltages applied to each element of the matrix and are not "power supply voltages for the circuit to the matrix element" as substantially recited in each of claims 1 and 12.

Sato is clear that the (emphasis added) "two nMOS structure TFTs 6 and 7 are connected between two adjacent data lines 1-na, 1-nb ..." (See, Sato, Col. 9, lines 45-46.) Sato explains that "[f]irst, the potential of the scanning line 2-n (n: a natural number indicative of the number of rows of the scanning lines) corresponding to the pixel to be written is raised to high level. Therefore, the two TFTs 6 and 7 connected between the two data lines 1-na and 1-nb of the n-th row which corresponds to the scanning line 2-n are both turned on." "Under these conditions, a video signal is transmitted through the two data lines 1-na and 1-nb. In this case, the video signals transmitted to the two data lines 1-na and 1-nb are mutually opposite in phase to each other.

Under these conditions, **the two video signals are written from the two data lines 1-na and 1-nb in the digital memory cell 100** composed of the two inverters elements 4 and 5. In this case, in order to enable the data to be written in the digital memory cell 100, it is necessary to increase the driving capability of the entire data line drive circuit system including the two TFTs 6 and 7 higher than that of the two inverter elements 4 and 5." (See, Sato, Col. 11, lines 49-67.)

The Final Office Action in relying on how Sato shows first and second column conductors supplying first and second voltages, refers not to the "two data lines 1-na and 1-nb" cited in the Final Office Action as corresponding to the first and second column conductors of the claims of the present application, but in fact, refers to the data line 1-1 and the scan line 2-2 (see, Sato, FIG. 1, and the Final Office Action, page 3, paragraph 2).

Accordingly, while Sato shows writing data voltage via the "two data lines 1-na and 1-nb", Sato does not show the first and second column conductors providing power supply voltages for the circuit to the matrix element.

This apparently is undisputed, notwithstanding the position forwarded on page 3, paragraph 2 of the Final Office Action discussed above, since the Final Office Action acknowledges that "Sato fails to expressly teach providing power supply voltages for the circuit to the matrix element in second time periods

interspersed between the first time periods." (See, Final Office Action, page 3, paragraph 3.)

Aoki is cited to provide that which is admitted missing from Sato, however, it is respectfully submitted that reliance on Aoki is misplaced.

While Aoki, FIG. 5 does show a single pre-charge signal interspersed with a single data signal per pixel element, it is respectfully submitted that this is not all of what is admitted by the Final Office Action as missing from Sato.

While the Final Office Action has elected to focus on the timing portion of the claims with reference to Aoki, namely, power supply voltages ... interspersed between the first time periods, it is respectfully submitted that claim 1, for example, recites that the (emphasis added) "plurality of first and second column conductors, each arranged for inputting data signals to or outputting data signals from the matrix elements of a respective column in first time periods, and each arranged for providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods ..."

It is respectfully submitted that it is the (emphasis added) "present inventors [of the presently pending application that] have realized it would be advantageous to provide power supply voltages to circuits within matrix array elements by using the same column conductors that are used for supplying data to the array elements

... or extracting or outputting data from matrix array elements ..." (See, present application, page 2, lines 8-15.)

It is respectfully submitted that the active matrix array of claim 1 is not anticipated or made obvious by the teachings of Sato in view of Aoki. For example, Sato in view of Aoki does not teach, disclose or suggest, an active matrix array that amongst other patentable elements, comprises (illustrative emphasis added) "a plurality of first and second column conductors, each arranged for inputting data signals to or outputting data signals from the matrix elements of a respective column in first time periods, and each arranged for providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods, wherein the first column conductors supply first voltage and the second column conductors supply second voltage to each matrix element and wherein the first voltage and the second voltage are separate voltages" as recited in claim 1, and as similarly recited in claim 12.

It is respectfully submitted that neither of Sato nor Aoki teach, disclose or suggest the first and second column conductors inputting/outputting data signals to/from the matrix elements of a respective column and providing power supply voltages for the circuit to the matrix element.

Based on the foregoing, the Applicant respectfully submits that independent claims 1 and 12 are patentable over Sato in view of Aoki and notice to this effect is earnestly solicited. Claims

2-11 respectively depend from claim 1 and, accordingly, are allowable for at least this reason as well as for the separately patentable elements contained in each of these claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

In addition, Applicant denies any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicant reserves the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

Applicant has made a diligent and sincere effort to place this application in condition for immediate allowance and notice to this effect is earnestly solicited.

Respectfully submitted,

By _____

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